Claims

1. A microelectromechanical device ~~having~~ comprising at least one thermoelectric layer on a substrate~~, in particular a thermoelectric layer on a substrate~~,

wherein ~~the~~ a thermal expansion coefficient of said at least one thermoelectric layer ~~and the~~ differs greatly from a thermal expansion coefficient of the substrate ~~differing greatly~~, and

wherein said at least one thermoelectric layer ~~(1)~~ is coupled to at least one stress reduction means ~~(2)~~ for the targeted reduction of lateral mechanical stresses present in the layer ~~(1)~~.

2. The microelectromechanical device as claimed in claim 1, wherein at least one stress reduction means ~~(2)~~ is arranged between regions of at least one of a functional structure and~~/or~~ a region with a thermoelectric layer ~~(1)~~.

3. The microelectromechanical device as claimed in claim 1 ~~or 2~~, wherein at least one region of the substrate ~~(10)~~ has an antiadhesion layer ~~(4)~~ for reducing or preventing the adhesion of material of the layer ~~(1)~~ and thus for forming at least one stress reduction means ~~(2)~~.

4. The microelectromechanical device as claimed in claim 3, wherein the antiadhesion layer ~~(4) has a Ti-W alloy or SiO_2 or~~ comprises at least one of Ti-W alloy ~~or~~and SiO_2.

5. The microelectromechanical device as claimed in ~~at least one of the preceding~~ claims 1, wherein a vertical offset between two laterally adjoining layers ~~(1)~~ is arranged as said stress reduction means ~~(2)~~ in at least one region on the substrate ~~(10)~~.

6. The microelectromechanical device as claimed in claim 5, wherein the vertical offset is formed by a prestructuring of the substrate ~~(10), in particular with~~ using at least one of an electrode metal ~~(5)~~ and~~/or~~ an adhesion layer ~~(3)~~.

7. The microelectromechanical device as claimed in ~~at least one of the preceding~~ claim~~s~~ 1, wherein at least one ~~mechanically and/or chemically introduced~~ trench is arranged as said stress reduction means ~~(2)~~ in at least one region of the substrate ~~(10)~~.

8. The microelectromechanical device as claimed in claim 7, wherein at least one trench has a depth of up to 100 µm.

9. The microelectromechanical device as claimed in ~~at least one of the preceding~~ claim~~s~~ 1, wherein the difference between the thermal expansion coefficient of at least one layer ~~(1)~~ and the thermal expansion coefficient of the substrate ~~(10)~~ is at least $3 * 10^{-6}$ K^{-1}~~, in particular at least 10^{-5} K^{-1}~~.

10. The microelectromechanical device as claimed in claim 9, wherein the difference between the thermal expansion coefficient of at least one layer and the thermal expansion coefficient of the substrate is at least 10^{-5} K^{-1}.

~~10~~11. The microelectromechanical device as claimed in ~~at least one of the preceding~~ claim~~s~~ 1, wherein the layer thickness of ~~a~~ said thermoelectric layer ~~(1)~~ is ~~between~~ in the range of 2 and 100 µm.

~~11~~12. The microelectromechanical device as claimed in claim ~~10~~11, wherein the layer thickness is ~~between~~ in the range of 20 and 100 µm.

~~12~~13. The microelectromechanical device as claimed in ~~at least one of the preceding~~ claim~~s~~ 1, wherein the substrate ~~(10) at least partly~~ comprises at least one of mica, glass, BaF_2, silicon, silicon dioxide, silicon carbide and~~/or~~ diamond.

~~12. The microelectromechanical device as claimed by at least one of the preceding claims, featuring at least one semiconductor component composed of two substrates (10).~~

~~12~~14. The microelectromechanical device as claimed in ~~by at least one of the preceding~~ claim~~s~~ 1, ~~featuring~~ wherein said thermoelectric layer forms at least one of a Peltier element and~~/or~~ a thermogenerator element.

~~13~~15. The microelectromechanical device as claimed in ~~at least one of the preceding~~ claim~~s~~ 1, wherein the thermoelectric layer ~~(1) has a proportion of typical~~ comprises a thermoelectric material~~, in particular~~including at least one of Bi_2Te_3, PbTe, SiGe and~~/or~~ skutterrudite.

~~14~~16. A method for producing a ~~microelectromechanical device as claimed in claim 1, in particular a~~ thermoelectric semiconductor component, the method comprising

~~wherein~~

forming a layer ~~(1)~~ on a substrate ~~(10)~~such that the layer is coupled to at least one stress reduction means ~~(2)~~ for the targeted reduction of lateral mechanical stresses present in the layer ~~(1)~~.

1~~5~~7. The method as claimed in claim 1~~4~~6, wherein forming the layer comprises forming a thermoelectric layer, and wherein the method further comprises arranging said at least one stress reduction means ~~(2) is arranged~~ between regions of at least one of a functional structure and~~/or~~ a region with a thermoelectric layer~~ (1)~~.

1~~6~~8. The method as claimed in claim 16~~4 or 15~~, ~~wherein~~further comprising forming an antiadhesion layer ~~(4)~~ for reducing or preventing the adhesion of material of the layer~~ (1)~~ and thus for forming at least one stress reduction means~~ (2) is grown~~ in at least one region of the substrate~~ (10)~~.

1~~7~~9. The method as claimed in ~~at least one of~~ claim~~s 14 to~~ 16, ~~wherein~~ further comprising arranging a vertical offset between two laterally adjoining layers ~~(1) is arranged~~ as said stress reduction means~~ (2)~~ in at least one region on the substrate~~ (10)~~.

~~18~~20. The method as claimed in ~~at least one of~~ claim~~s~~ 16~~4 to 17~~, ~~wherein~~ further comprising producing at least one trench ~~is produced~~ using at least one of mechanical~~ly~~ and~~/or~~ chemical~~ly~~ processes as said stress reduction means~~ (2)~~ in at least one region of the substrate~~ (10)~~.

21. A microelectromechanical device comprising:

a substrate having a first thermal expansion coefficient; and

a thermoelectric layer formed over the substrate, the thermoelectric layer having a second thermal expansion coefficient that differs from the first thermal expansion coefficient by at least 10^{-5} K^{-1};

wherein said at least one thermoelectric layer is divided into a plurality of thermoelectric layer portions, each thermoelectric layer portion being separated from adjacent thermoelectric layer portions by a stress reduction region, and

wherein said each thermoelectric layer portion has a thickness in the range of 2 and 100 μm, and an width in the range of 1.4 to 20 mm.